

The TOTEM Roman Pot Electronics System

G. Antchev *

On behalf of the TOTEM Collaboration

* INRNE-BAS, Sofia, Bulgaria

Gueorgui.Antchev@cern.ch

Abstract

The TOTEM experiment has three sub-detectors: Roman Pots (RP) with silicon strips, the T1 detector with Cathode Strip Chambers (CSC) and T2 with Gas Electron Multiplier detectors (GEM). The RP detectors are located in the straight sections of the LHC tunnel on both sides of the CMS experiment at IP5. The TOTEM RP Electronics System consists of the following main components: the front-end with the VFAT2 chip mounted on the RP hybrids for tracking and trigger generation; the on-detector electronics based on the RP Motherboard (RPMB) for data conversion and transmission, and the counting room electronics with data acquisition and trigger systems based on the TOTEM Front End Driver (TOTFED). A detailed overview of the TOTEM Roman Pot Electronics System and its components is presented in this paper.

I. INTRODUCTION

TOTEM (Total Cross Section, Elastic Scattering and Diffraction Dissociation Measurements) [1] is an experiment dedicated to the measurement of total cross section, elastic scattering and diffractive processes at the LHC. The full TOTEM detector is composed of Roman Pot Stations (RPS), Cathode Strip Chambers T1 (CSC) and Gas Electron Multipliers T2 (GEM). The T1 and T2 detectors are located on each side of the CMS interaction point in the forward region, but still within the CMS cavern, see Figure 1.

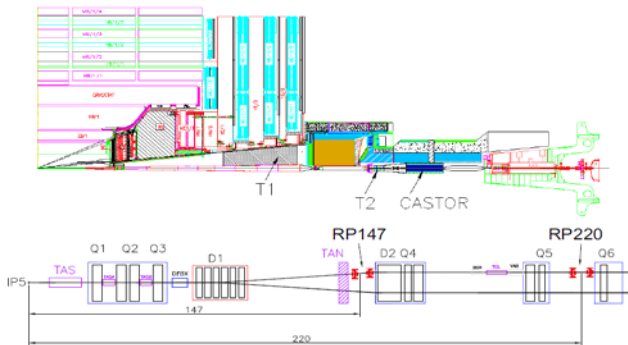


Figure 1: Top: The TOTEM forward detectors T1 and T2 embedded in the CMS detector. Bottom: The LHC beam line and the Roman Pots at 147m (RP147) and 220m (RP220) sector 5-6

Two Roman Pot (RP) stations are installed in the straight section of the LHC tunnel on each side of the interaction point at 220 m and 147 m. Each RP station consists of two groups of three RP separated by a few meters to obtain a sufficiently large lever arm to establish

co-linearity with the LHC beam for the tracks prior to generating a level 1 trigger for the corresponding event. Three Roman Pots were designed in one group to approach the beam with detector stacks from three different sides (top, bottom and one side, the other side is impossible due to the presence of the second beam pipe). Each RP contains 10 silicon strip detectors with 512 strips.

II. GENERAL DESIGN SPECIFICATIONS

TOTEM needs to operate both as a standalone experiment and as a sub-detector of CMS. This requires full compatibility with CMS. The RPs need to participate in the trigger building with a high degree of flexibility. All this requires the use of several CMS components. Standardization was necessary across the TOTEM sub-detectors for the integrated circuits development and the counting room hardware. This leads to similar systems for all three sub-detectors: they work with the same front end chips but with different front-end boards compatible with their specific channel segmentation and geometry.

III. SYSTEM OVERVIEW

Figure 2 shows the TOTEM RP Electronics System Basic Block Diagram.

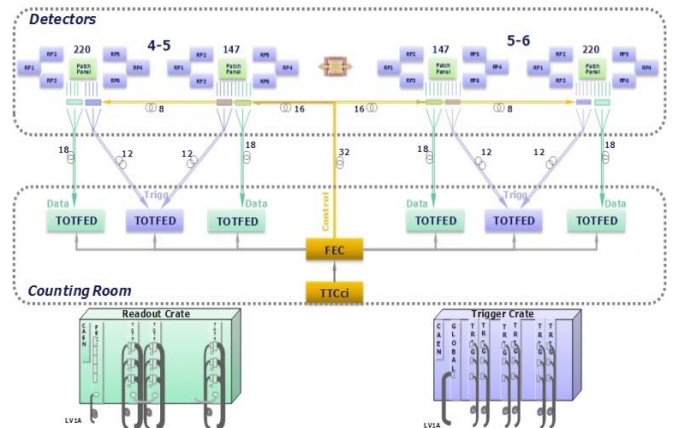


Figure 2: The TOTEM RP Electronics System Basic Block Diagram

The TOTEM RP Electronics system is divided physically in two levels: on-detector electronics and counting room electronics [2]. The on-detector electronics are in the tunnel and are electrically isolated from the counting room via floating power supplies, optical signal transmission and electrical transmitters with optocouplers. Due to the radiation requirements, the low voltage power supplies are located in the closest alcove in the tunnel up

to 70 m from the RP. The high voltage power supplies are located in the counting room. The two levels of the system are more than 200m apart.

IV. ON-DETECTOR ELECTRONICS

In the following section, the system will be described in more detail starting from the on-detector electronics and moving up to the counting room electronics.

A. VFAT 2 readout chip

The VFAT2 front end ASIC [3] provides tracking and trigger building data. The VFAT2 chip provides binary tracking data (1 bit per channel and per event). All data corresponding to a triggered event is transmitted without zero suppression. The ~160 8 bit registers controlling the VFAT2 chip are programmable through its I2C interface. The VFAT2 includes a counter on its fast trigger outputs to monitor hit rates. Figure 3 presents a photo of the chip.

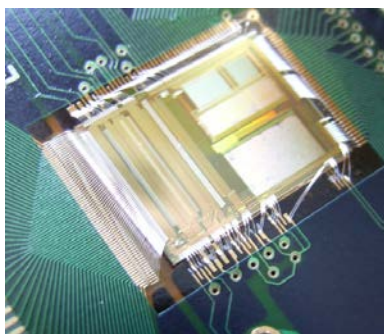


Figure 3: The VFAT 2 chip

B. The Silicon Detector Hybrid

The silicon detector hybrid (Figure 4) carries detector and 4 VFAT2 readout chips and a Detector Control Unit DCU chip. The hybrid is connected to the outside world by means of an 80 pin connector linked to a flat cable. The VFAT2 is biased internally - so as to simplify the design of the hybrid.



Figure 4: The Silicon Detector Hybrid

Each VFAT2 will send 4 trigger outputs to the motherboard for further coincidence, resulting in 16 trigger outputs per hybrid (so 32 wires for LVDS occupying 40 % of the connector). The connector linking the hybrid to the motherboard carries also HV and LV power, clock and trigger signal, and also connections PT100 for temperature control. The strips on the detector form a 45 degrees angle with the edge close to the beam. Flipping the detector hybrid and mounting it face-to-face with the next one result in orthogonal strips giving the U

and V coordinate information. A picture of the detector package is shown on Figure 5.

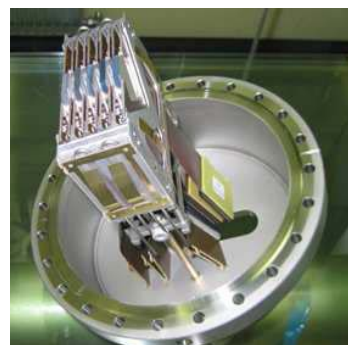


Figure 5: Detector package

All electrical components are mounted on one side (the right looking from the top) to avoid losing space between the hybrids.

C. The Roman Pot Motherboard

The TOTEM Roman Pot Motherboard (RPMB) [4] is the interface between the hybrids with silicon detectors and front end chips in the Roman Pots, and the outside world. The RPMB is glued in the vacuum flange which separates the vacuum chamber containing the detector hybrids, and forms the feed through between vacuum and atmosphere. The hybrids have a flexible part with an on-board connector for connection to the motherboard. The motherboard is equipped with connectors to the detector hybrids from one side and front panel with connectors to the patch panel from the other side.

The RPMB needs to provide power and control, as well as clock and trigger information to the 10 hybrids. It acquires tracking and triggers data from the hybrids, performs data conversion from electrical to optical format and transfers the data to the next level of the system. It also collects information such as temperature, pressure and radiation dose inside the pot. Figure 6 shows a picture of the RPMB and mezzanines and on Figure 7 is presented the functional block diagram.

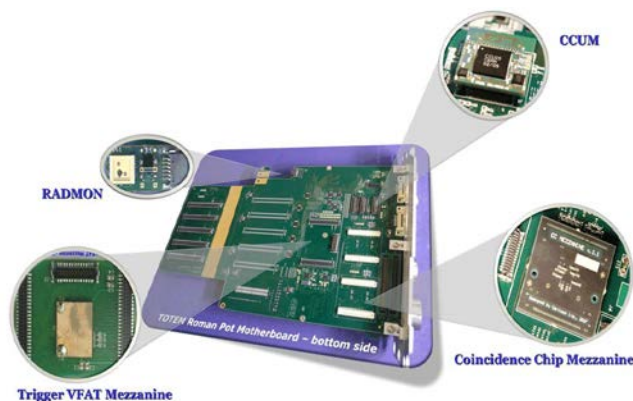


Figure 6: The picture of the RPMB and mezzanines

Apart from the electrical functionality described in detail below, the design of the RPMB was constrained by the mechanics and by radiation tolerance.

The RPMB has to fit in the Roman Pot mechanics, connect to 10 hybrids in a secondary vacuum (the primary vacuum is that of the machine within the beam pipe, the primary and secondary vacuum are separated by a window of about 100 micron thick), and feed through about 800 signals to and from the outside world. The connections to the outside are naturally on the end opposite to the hybrids. The maximum width of the feed through for these 800 signals is about 12 cm and together with the other size limitations this results in a very challenging layout with 16 layers for the RPMB.

The RPMB is also subject to radiation, requiring all components to be radiation tolerant. In particular, all on-board integrated circuits are full-custom circuits designed in 0.25 micron CMOS technology with special techniques to increase the radiation tolerance [5][6].

The board also had to be produced in halogen free material because of safety regulations.

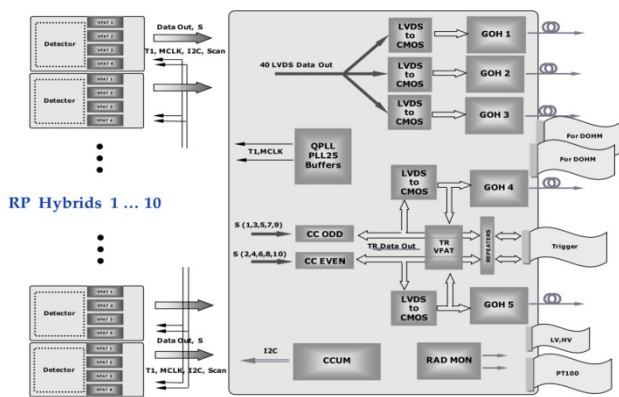


Figure 7: The RPMB Functional Block Diagram

The following are the general building blocks of the motherboard: Clock and Trigger distribution circuitry, Gigabit Optical Hybrids (GOH) – three for data and two for trigger bits transfer, two Coincidence Chip mezzanines, LVDS to CMOS converters, Trigger VFAT2 mezzanine, Control Unit mezzanine CCUM, Radiation Monitor circuitry and temperature sensors.

1) Power Distribution

The RPMB needs to receive low voltage power at 2.5 V for its own operation, and for the operation of the hybrids. The power on the hybrids has been carefully separated between analogue and digital blocks, both powered at 2.5 V.

The silicon detectors need to be biased up to 500 V after irradiation. The RPMB receives this high voltage supply and distributes it to the detector hybrids. The supply is separate for all detectors; grouping is done in the counting room. This allows isolating defective detectors from the rest if needed.

2) The slow control

The slow control system is the same as for the CMS Tracker and ECAL detectors [7]. A FEC-CCS board in the counting room sends and receives optical control data. A Digital Opto-Hybrid Module (DOHM) converts this data back to electrical form and interfaces with the RPMB via two 20pins 3M high speed connectors placed on the front panel.

A Communication and Control Unit mezzanine (CCUM) on the RPMB (see Figure 8) decodes this information and provides 16 I²C interface channels and one 8 bit parallel control port for use on the RPMB. All integrated circuits including the VFAT2 are controlled using these I²C interfaces.

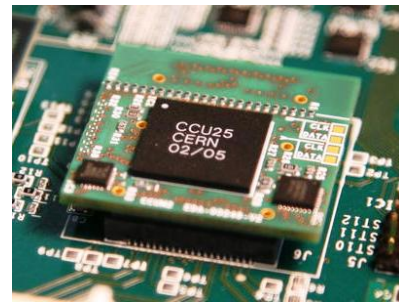


Figure 8: CCUM Mezzanine photo

In addition to the slow control information transmitted over I²C, several sensors mounted on the RPMB or on the hybrids provide additional information like temperature, pressure and radiation dose data.

PT100/1000 sensors are used for temperature, and a piezoelectric pressure sensor measures the pressure inside the pot.

A special small carrier card (RADMON) [8] is used for radiation monitoring on the RPMB. This carrier is made of a thin (~500 m) double-sided PCB. It can host up to 5 *p-i-n* diodes and five RadFETs mounted inside a proper package. It also includes a temperature sensor (10k NTC). A photo of the carrier is shown on Figure 9.

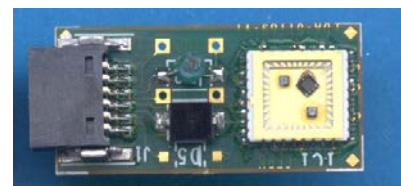


Figure 9: RADMON carrier photo

3) Clock and Fast Commands

The FEC-CCS card receives clock and fast commands in the counting room and includes these with the slow control data for transmission to the detector using the same channel as the slow control. On the RPMB, the clock and fast command signals are reconstructed by the PLL25 chip. The QPLL, a quartz based PLL, is used to further reduce the clock jitter necessary for serialization and optical transmission of data. The clock and fast command tree has been designed to minimize timing spread over all components on the RPMB.

4) Tracking Data transmission

The data sent by the VFAT2 front end chips upon a level 1 trigger signal is converted from LVDS to CMOS on the RPMB and then presented to the gigabit optical hybrids GOH modules, which serialize and convert the electrical data to optical for transmission to the Data Acquisition (DAQ) system in the counting room. Three GOH modules are used to send data from 40 VFAT2 chips.

5) Trigger Data generation and Transmission

Each VFAT2 front end chip has 8 trigger outputs, 4 of which are used in the Roman Pots. Every hybrid therefore generates 16 trigger outputs, and 5 hybrids have the same orientation of the silicon strips (U coordinate), and the 5 others have strips oriented at 90 degrees (V coordinate). The trigger signals are put into coincidence using two separate Coincidence Chips (CC) - one for the U and one for the V coordinate. The CC chips are mounted on the RPMB as mezzanine cards (CC mezzanine), one mezzanine per CC. Figure 10 shows a photo of the CC mezzanine.

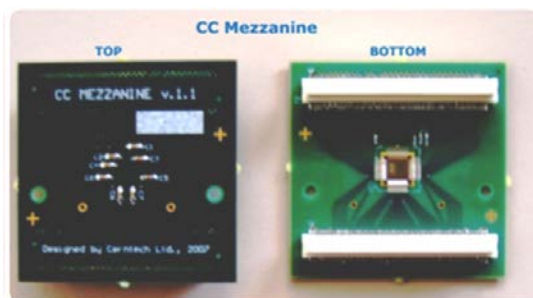


Figure 10: CC Mezzanine photo

The CC provides 16 outputs (so the number of trigger signals is reduced from 2×80 to 2×16), and these signals have to be transmitted to the counting room.

For these coincidences a full custom chip was developed instead of using a Field Programmable Gate Array. There are two reasons for this:

- The latency constraints on the generation of the trigger bits (especially from the Roman Pots) are very severe: after subtraction of cable delays, only about 8-10 bunch crossings are left for the generation of the trigger signals to be provided to CMS from the signals generated by the Roman Pot. A full custom chip with dedicated logic can implement the required coincidence in one clock;

- The CC needs to be placed on the RPMB or at least near the detectors and is therefore subject to radiation. Special design techniques were used to make the CC much more robust against radiation both with regard to total dose and single event effects than a standard FPGA. The CC mezzanine was designed to carry one Coincidence Chip and two 130 pins input/output connectors.

To transmit trigger bits to the counting room two ways have been selected: optical fibres are used for the 147m RP stations and in TOTEM standalone runs also for the

220m stations. The runs with CMS on the other hand are subject to CMS's limited trigger latency time, imposing trigger bit transmission with LVDS signals through fast electrical cables, because the serialization and deserialization and optical transmission in the fibre (~ 5 ns/m) take too much time. The electrical transmission over such a long distance requires a lot of care to preserve signal integrity. This can only be achieved by restoring the LVDS signals to full levels at regular intervals over the transmission distance. A special integrated circuit was designed for this purpose: the LVDS repeater chip can treat 16 LVDS channels in parallel and was designed in a special layout to guarantee radiation tolerance. This chip is mounted on a small repeater board. A repeater stations consists of 12 repeater boards (one for every cable carrying 16 LVDS signals) are placed at regular intervals of about 70m.

Since the trigger signals are sent on every clock cycle, some time reference has to be included in the trigger data stream to facilitate recovering the correspondence between the event and the transmitted bits. This is achieved through the VFAT2 trigger mezzanine which is set to receive the fast command bunch crossing 0 (BC0) and generate the corresponding output (Figure 11). As a result, the GOH's data valid signal is disabled upon reception of the BC0 signal for the duration of one clock cycle. This can be recognized in the counting room, and provides the time reference.



Figure 11: Trigger VFAT2 Mezzanine

In addition, the VFAT2 trigger mezzanine records the trigger bits and merges them upon a level 1 trigger with the tracking data, so that the trigger bits which lead to a triggered event are recorded with the tracking data from that event.

D. Digital Opto Hybrid Module

The control, timing and trigger information per RP station is handled by one TTC ring which follows the CMS standard. A Digital Opto Hybrid Module (DOHM) receives and sends the optical information using two Digital Opto Hybrids (DOH) mezzanines. It converts these optical signals from and to electrical signals for the token ring. A photo of the DOHM module is presented on Figure 12.

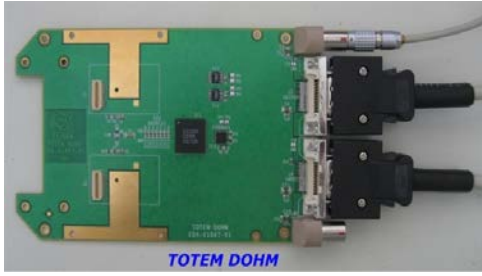


Figure 12: DOHM photo

V. COUNTING ROOM ELECTRONICS

The counting room electronics have been fully standardized across all TOTEM detectors and the same hardware is used for data readout and trigger signal generation.

A. The TOTEM Front End Driver

The TOTEM Front End Driver, so-called TOTFED, receives and handles trigger building and tracking data from the TOTEM detectors, and interfaces to the global trigger and data acquisition systems. The TOTFED is based on the VME64x standard and has deliberately been kept modular [9].

The TOTEM Front End Driver (TOTFED) functional blocks are shown on Figure 13. The general blocks are: Optical Receiver Modules (OptoRX12); CMC Transmitter, based on the S-Link64 interface; VME64x Interface; USB Interfaces; MAIN and MERGER Controllers with associated SPY Memory Buffer and Clock distribution circuits.

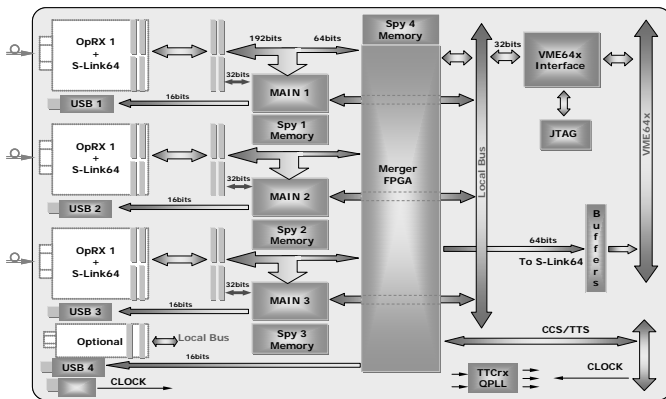


Figure 13: TOTFED Functional Block Diagram

The CMS ECAL group has developed the Data Concentrator Card (DCC) [10]. The board has 72 optical 800 Mbit/s inputs implemented in 6 NGK 12-Channel Receivers.

This board is very close to the full GOL count for the Roman Pots (72) and about twice the GOL count of the GEM detectors. However, the data and trigger information content of the TOTEM GOLs is much higher: the TOTEM data density is such that only 9 optical channels would completely saturate one Slink64, thus requiring one DCC for each 9 channels – an extremely inefficient solution. A

new module has therefore been designed using the previous development as much as possible.

1) Design Strategy and Components

The TOTFED has been designed as a modular device. It is built from a set of mezzanine cards plugged onto a main motherboard known as the “VME64x Host Board”.

The expensive optical components are mounted solely on mezzanine cards, so that they can be tested separately and preserved if the motherboard is defective. Motherboards can be equipped with a fraction of the total number of mezzanines, and some of the mezzanines can be different depending on the application. For example, the base configuration for the CMS Preshower application has three OptoRX12 mezzanines associated to a single S-Link64 (and FRL) but it is possible to incorporate a further mezzanine card to aid data suppression prior to the S-Link64 [12]. For the TOTEM application the incoming data is distributed over three FRLs. The TOTFED is intended for operation in a VME environment in the experiment but is also equipped with USB ports to allow standalone operation. This is being implemented on the basis of previous CMS Preshower work [13]. A photo of the TOTFED is presented in Figure 14.

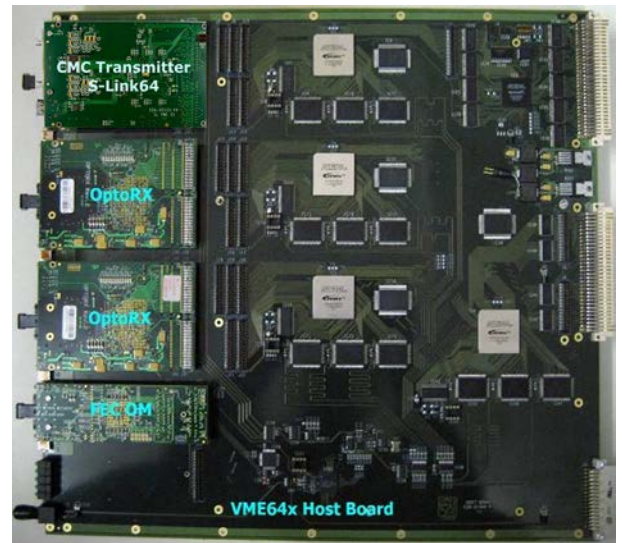


Figure 14: TOTFED photo

2) VME64x Host Board

The VME64x Host Board is in 9U VME64x format. It is a motherboard that accepts different mezzanine modules. It has PMC connectors for three OptoRX12 modules and three other sets of PMC connectors for optional use. The MAIN and MERGER functional blocks are implemented in FPGAs from the Altera Stratix family. Every OptoRX12 has its associated MAIN controller connected via a 192bit bus. The MERGER shares part of this bus: 64bits from each MAIN controller. The VME64x Interface is implemented in a further FPGA from the Altera Cyclone family and is configured as a bridge between the VME and Local Bus.

The VME64x Host Board includes the TTCrx [14] ASIC with associated chipset for receiving the TTC

signals and distributing the decoded information across the board. The TTC signals are provided to the TTCrx optically and/or electrically. For the optical interface with the TTCrx, an associated optical receiver is used. Concerning the electrical interface, an additional connector in the back side of the card is used. The same connector is used to provide an extra flag that signals possible buffer overflow (trigger throttling signal). On top of every OptoRX12 it is possible to plug-in a dedicated CMC Transmitter module, which connects the TOTFED to the DAQ system. There is also a possibility to connect a fourth CMC Transmitter module to the VME J2 connector and additional rear adapter.

Flexible JTAG programming interface is used for reconfiguring all the on-board FPGAs (in a variety of ways), including those hosted by the mezzanine modules.

3) The OptoRX12 module

The OptoRX12 is a general purpose plug-in module used for reception of optically transmitted data by gigabit applications. It is based on a 12-channel optical receiver and an FPGA from the Altera Stratix GX family with embedded hardware de-serializers qualified for data rates up to ~ 3.2 Gbps. The FPGA embedded de-serializers are compatible with the Gigabit Ethernet protocol/encoding. For the interconnection with the VME64x Host Board, the module incorporates an electrical interface (using five 64-pin PMC type connectors). The electrical interface comprises dedicated pins for powering, clocking, configuration via JTAG as well as a large number (280) of lines driven from the FPGA's I/O pins. This large number of lines provides the de-serialized data from all 12 channels in parallel. Although the total number of interconnections is large, the physical dimensions of the OptoRX12 were kept relatively small (115mm x 75mm) allowing up to three of these modules to be plugged into a VME64x Host Board (340mm x 360mm). Figure 15 shows a photograph of the module. Details about the OptoRX12 can be found in [11].



Figure 15: The OptoRX12 mezzanine module

B. The RP DAQ System

The RP Data Acquisition System (DAQ) is built around the TOTFED unit. The main objectives of this system are to acquire on-detector data from up to 72 optical links, perform on-line data formatting and pass the data to the second level of the system. The DAQ also is used for initialization and calibration of the front-end VFAT2 chips. It is meant to operate in two modes – stand-alone data taking at up to ~ 1 KHz and data taking

integrated in the CMS DAQ system at a later stage. In the stand-alone mode the VME64x at ~ 40 MB/s is being used to read out the data from the detectors, while in data integrated with CMS mode the S-Link64 interface is being used at the higher rate of ~ 200 MB/s. The total amount of Si detectors to be read is 240 and the number of channels is 122880, which is covered by 960 VFAT2 chips.

Four TOTFED units are mounted in one crate together with the Front-End Controller (FEC) and Trigger and Timing Control (TTCci) units. The photo of the RP DAQ crate is shown on Figure 16.



Figure 16: The RP DAQ crate

The data from the crate is transferred to the TOTEM DAQ cluster. The cluster is a set of PCs for event building and storing. The rates and capacities are accommodated in present medium level storage and a transfer system based on Fibre Channel and SCSI technology.

C. The RP Trigger System

As it was mentioned above, the second function of the VFAT2 - triggering is to provide programmable “fast OR” information based on the region of the sensor hit. This can be used for the creation of a level 1 trigger. The Sector outputs (S-bits) of the VFAT2 give the result of internal fast OR operations within one clock cycle. These S-bits are in LVDS format. A Coincidence chip then performs coincidence operations between VFAT sector outputs.

The outputs from the CC chip (still in LVDS format) are then converted to CMOS levels by dedicated LVDS-to-CMOS converters. Using the GOH, the trigger data is then serialized and transmitted at 800 Mb/s to the counting room. The VME64x Host Board equipped with OptoRX12 receivers and additional mezzanines compose the trigger system. After converting to electrical signal, the trigger information is analyzed in the onboard FPGAs and it is transferred to the local global trigger generator board LONEG. This is a mezzanine board plugged onto another VME64x Host Board to build so called Trigger TOTFED. Since the same hardware and software are being used to readout the Trigger TOTFED, it is easy to integrate the trigger data into the data stream from the readout

TOTFED. The photo of the Trigger crate is shown on Figure 17.

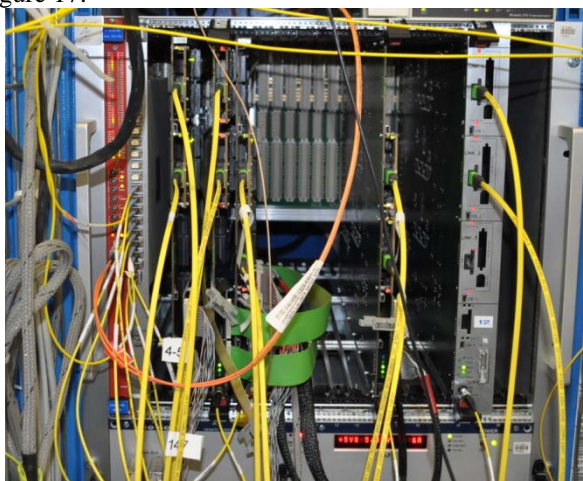


Figure 17: The TOTEM Trigger crate

In the Trigger TOTFED board inside the FPGA the complex algorithms can be performed in order to prepare the trigger primitives for the global L1 trigger.

The RP station RP220 is so far away from the counting room that optically transmitted trigger data would not arrive within the latency allowed by the trigger of CMS. Therefore, in addition to optical transmission for TOTEM runs, the electrical transmission with LVDS signals was implemented for common runs with CMS. To maintain the electrical isolation between the detector and the counting room, optocouplers are used to receive these electrically transmitted signals. At regular intervals of about 70m along the total cable length of 270 m, repeaters based on a custom-designed LVDS repeater chip are inserted to preserve the electrical signal quality.

VI. SUMMARY

The Roman Pot Electronics System was built on a modular principle and it is based on the common hardware and software developed within the frame of TOTEM collaboration. Using the same hardware in the counting room for tracking data and trigger building provides possibilities for common firmware developments. The system can be used in stand-alone mode and also in the CMS experiment. The proton-proton elastic scattering has been measured by TOTEM experiment at CERN in special dedicated runs with Roman Pot detectors using the described above electronics system. The results are presented in [15].

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